

What is claimed is:

1           1.     A structure for providing resilient interconnections in a wafer level  
2     package, comprising a conductive pad that overlays an air space, wherein at  
3     least a portion of the air space extends laterally beyond the conductive pad.

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1           2.     The structure as claimed in claim 1, wherein the air space  
2     comprises a geometric structure having a plurality of perimeter interconnect  
3     support structures for the conductive pad.

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1           3.     The structure as claimed in claim 2, wherein at least one perimeter  
2     interconnect support structure also supports a conductive line electrically  
3     connected to the conductive pad.

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1           4.     The structure as claimed in claim 3, wherein the conductive line is  
2     a metal wire.

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1           5.     The structure as claimed in claim 1, wherein a major axis of the air  
2     space is radial to a center of the wafer level package.

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1           6.     The structure as claimed in claim 1, wherein a major axis of the air  
2     space is not radial to a center of the wafer level package.

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1           7.     The structure as claimed in claim 2, wherein at least one perimeter  
2 interconnect support structure also supports a conductive line electrically  
3 connected to the conductive pad.

1           8.     The structure as claimed in claim 7, wherein the at least one  
2 perimeter interconnect support structure is positioned relative to a center of the  
3 conductive pad less than or equal to about 60 degrees of the major axis.

1           9.     A method for making a structure for providing resilient  
2 interconnections in a wafer level package, comprising the steps of:  
3                 A.   forming a cavity having a first area on a semiconductor  
4                 substrate;  
5                 B.   filling the cavity with a removable material;  
6                 C.   forming a conductive layer over the removable material;  
7                 D.   patterning the conductive layer to form a conductive pad;  
8                 E.   removing the removable material to form an air space below  
9                 the conductive pad; and  
10                F.   forming an interconnection material on the conductive pad,  
11 whereby at least a portion of the air space extends laterally beyond the  
12 conductive pad.

1           10.    The method as claimed in claim 9, wherein the removable material  
2 is planarized before forming the conductive layer.

1           11. The method as claimed in claim 10, wherein the planarization is  
2 carried out by either an etch-back process or a CMP process.

1           12. The method as claimed in claim 9, wherein the removable material  
2 is material selected from the group consisting of a monomeric material, a  
3 polymeric material, and an elastomeric material.

1           13. The method as claimed in claim 9, wherein the removable material  
2 is a B-stage-able material.

1           14. The method as claimed in claim 9, wherein the cavity is formed by  
2 depositing a dielectric layer and thereafter patterning the dielectric layer.

1           15. The method as claimed in claim 14, wherein the patterning of the  
2 dielectric layer is carried out using a photolithographic process.

1           16. The method as claimed in claim 9, wherein after forming the  
2 conductive layer, a dielectric layer is deposited over the conductive layer.

1           17. The method as claimed in claim 9, wherein after forming the air  
2 space, a protective layer is deposited on a top and bottom surface of the  
3 conductive pad.

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1           18.    The method as claimed in claim 17, wherein the protective layer is  
2    carried out by an electroless plating method.

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1           19.    The method as claimed in claim 18, wherein the protective layer is  
2    formed using a metal.

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1           20.    The method as claimed in claim 19, wherein the metal is selected  
2    from the group consisting of gold and nickel.

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